100G SFP112 LR1 10km Transceiver

FSS-SPO101-LR1C

Features

- Full-duplex transceiver modules
- 106.25Gb/s PAM4 transmitter and PAM4 receiver
- 106.25Gbps PAM4 based on a cooled EML TOSA transmitter
- 106.25Gbps PAM4 PIN Receiver
- Power consumption <3.5W
- Hot Pluggable SFP112 form factor
- Compliant with SFF-DD MSA,*CMIS*
- Maximum link length of 10km on G.652 SMF with KP-FEC
- Duplex LC connector
- Built-in digital diagnostic functions
- Operating case temperature: 0°C to +70°C
- +3.3V power supply
- RoHS compliant (lead free)

Applications

- 100G Lambda 100G LR1-10
- IEEE802.3cu

Description

The Fiberstamp Technologies FSS-SPO101-LR1C is a single-Channel, Pluggable, Fiber-Optic SFP112 for 53.125GBd PAM4 Ethernet Applications. It is a high performance module for short-range data communication and interconnect applications which operate at 106.25Gbps up to 10km over Single-Mode Fiber (SMF). The electrical interface uses a 20 contact edge type connector. The optical interface uses duplex LC receptacle. The optical interface uses a Duplex LC connector. The high performance cooled EML transmitter and high sensitivity PIN receiver provide superior performance for 100Gigabit Ethernet applications up to 10km links.

Block Diagram

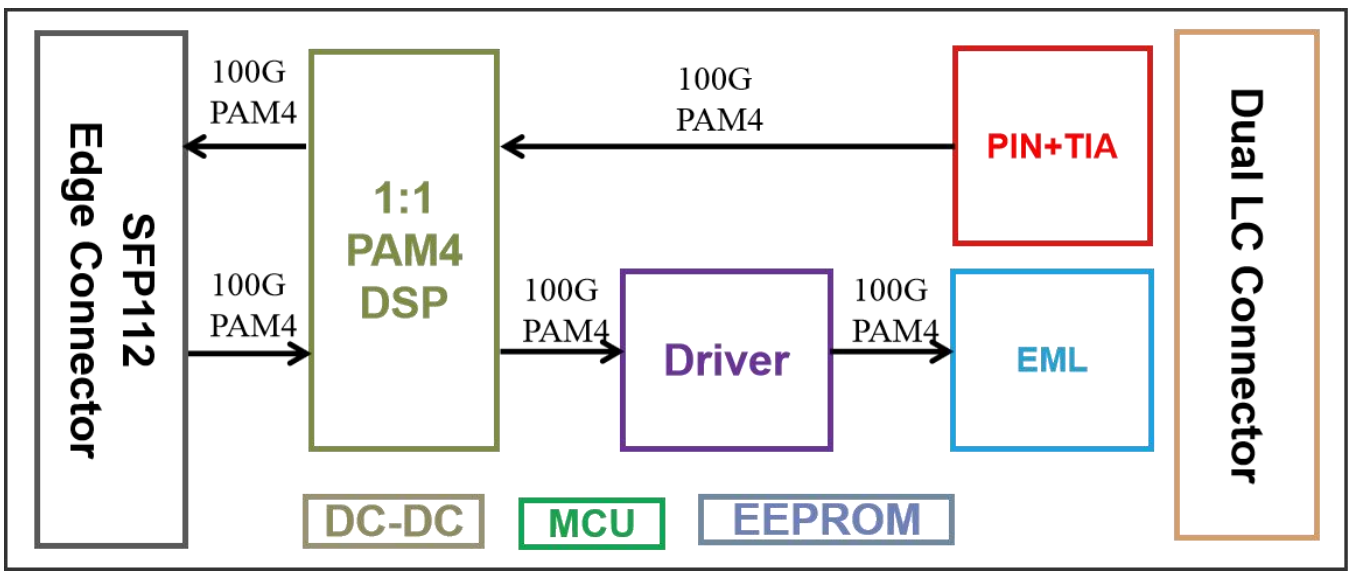


Figure1. Module Block Diagram

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage	Vcc	-0.3	3.6	V
Input Voltage	Vin	-0.3	Vcc+0.3	V
Storage Temperature	Tst	-20	85	°C
Case Operating Temperature	Top	0	70	°C
Humidity(non-condensing)	Rh	5	85	%

Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit
Supply Voltage	Vcc	3.13	3.3	3.47	V
Operating Case temperature	Tca	0		70	°C
Data Rate Per Lane	fd		53.125		GBd
Humidity	Rh	5		85	%
Power Dissipation	Pm		3	3.5	W
Link Distance with G.652	D			10	km

Electrical Specifications

Parameter	Symbol	Min.	Typical	Max.	Unit
Differential input impedance	Zin	90	100	110	ohm
Differential Output impedance	Zout	90	100	110	ohm
Differential input voltage Amplitude[1]	ΔVin	400		1600	mVp-p
Differential output voltage Amplitude[2]	ΔVout	-		900	mVp-p
Bit Error Rate	BER			2.4E-4	-
Input Logic Level High	VIH	2.0		Vcc+0.3	V
Input Logic Level Low	VIL	-0.3		0.8	V
Output Logic Level High	IOH	-50		37.5	uA
Output Logic Level Low	VOL	-0.3		0.4	V

Note：

1. Differential input voltage amplitude is measured between TD+ and TD-.
2. Differential output voltage amplitude is measured between RD+ and RD-.

Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Transmitter						
Centre Wavelength	λc	1304.5	-	1317.5	nm	-
Side-mode suppression ratio	SMSR	30	-	-	dB	-
Average launch power	Pout	-1.4	-	4.5	dBm	-
Optical Modulation Amplitude (OMAouter)	OMA	0.7		4.7	dBm	-
Transmitter and dispersion eye closure for PAM4(TDECQ)	TDECQ			3.4	dB	
Extinction Ratio	ER	3.5	-	-	dB	-
Average launch power of OFF transmitter				-30	dB	-

Receiver						
Centre Wavelength	λc	1304.5	-	1317.5	nm	-
Receiver Sensitivity in OMA outer for TECQ≤1.4dB for 1.4＜TECQ≤3.4dB	RXsen			-6.1 -7.5+ TECQ	dBm	1
Stressed Receiver Sensitivity in OMA outer	SRS			-4.1	dBm	2
Maximum Average power at receiver				4.5	dBm	-
Minimum Average power at receiver		-7.7			dBm	
Receiver Reflectance				-26	dB	-
LOS Assert	LOSA		-13		dBm	-
LOS De-Assert – OMA	LOSD		-11		dBm	-
LOS Hysteresis	LOSH	0.5			dB	-

Note：

1. Measured with conformance test signal at TP3 for BER = 2.4E-4 Per-FEC.
2. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

Diagnostics Specification

Parameter	Range	Unit	Accuracy	Calibration
Temperature	0 to +70	°C	±3°C	Internall
Voltage	3.0 to 3.6	V	±3%	Internal
Bias Current	0 to 120	mA	±10%	Internal
TX Power	-1.4 to +4.5	dBm	±3dB	Internal
RX Power	-7.7 to +4.5	dBm	±3dB	Internal

Digital Diagnostic Monitoring Interface

The transceivers provide serial ID memory contents and diagnostic information about the present operating conditions by the 2-wire serial interface (SCL, SDA).

The diagnostic information with internal calibration or external calibration all are implemented, including received power monitoring, transmitted power monitoring, bias current monitoring, supply voltage monitoring and temperature monitoring.

Memory Structure and Mapping

This limits the management memory that can be directly accessed by the host to 256 bytes, which is divided in Lower Memory (addresses 00h through 7Fh) and Upper Memory (addresses 80h through FFh).

A larger addressable management memory is required for all but the most basic modules. This is supported by a structure of 128-byte pages, together with a mechanism for dynamically mapping any of the 128-byte pages from a larger internal management memory space into Upper Memory the host addressable space.

The addressing structure of the additional internal management memory is shown in Figure 4 The management memory inside the module is arranged as a unique and always host accessible address space of 128 bytes (Lower Memory) and as multiple upper address subspaces of 128 bytes each (Pages), only one of which is selected as host visible in Upper Memory. A second level of Page selection is possible for Pages for which several instances exist (e.g. where a bank of pages with the same Page number exists).

This structure supports a flat 256 byte memory for passive copper modules and permits timely access to addresses in the Lower Memory, e.g. Flags and Monitors. Less time critical entries, e.g. serial ID information and threshold settings, are available with the Page Select function in the Lower Page. For more complex modules which require a larger

amount of management memory the host needs to use dynamic mapping of the various Pages into the host addressable Upper Memory address space, whenever needed.

Note: The management memory map has been designed largely after the QSFP memory map. This memory map has been changed in order to accommodate 1 electrical lanes and to limit the required memory space. The single address approach is used as found in QSFP. Paging is used in order to enable time critical interactions between host and module.

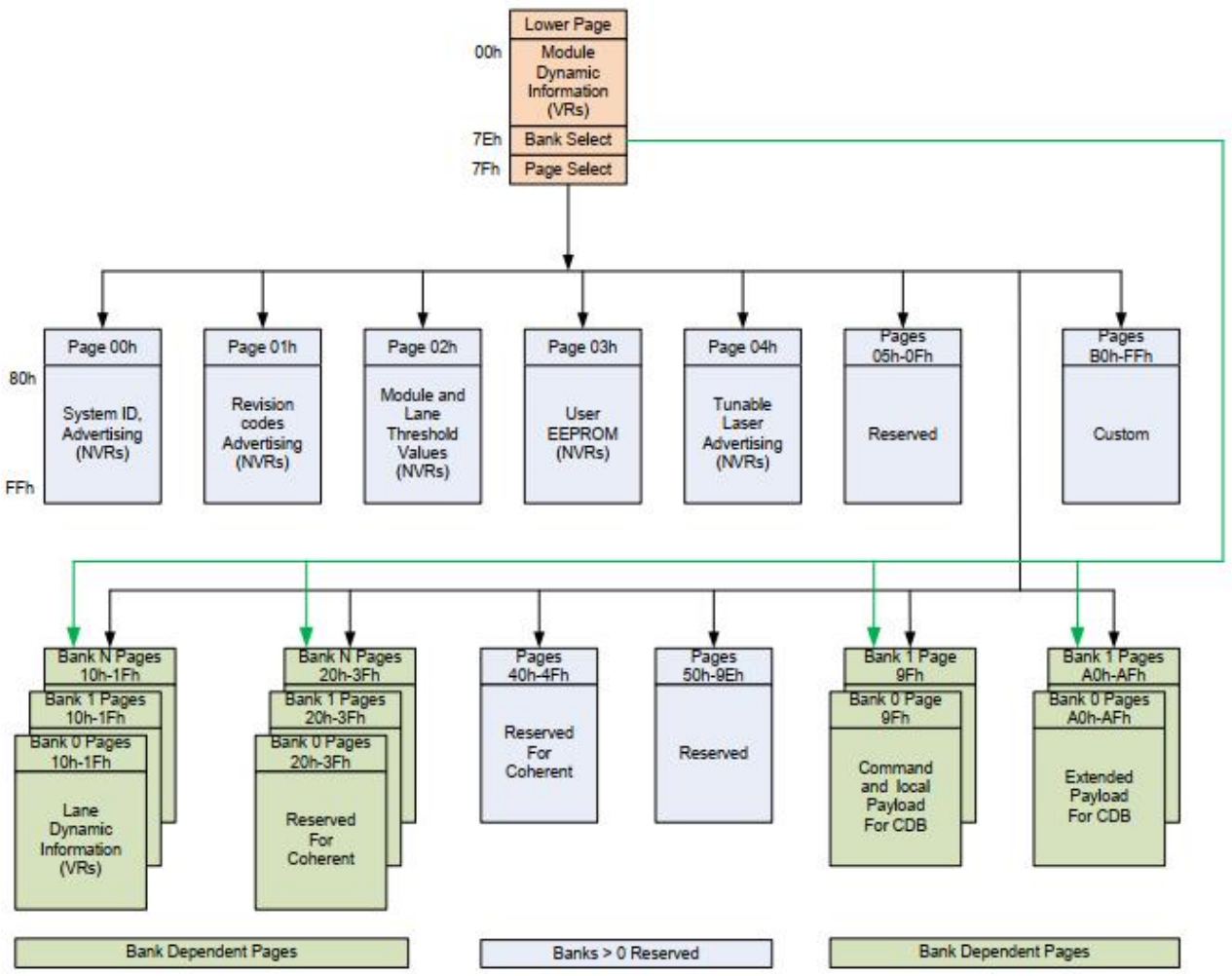
Supported Pages

A basic 256 byte subset of the Management Memory Map is mandatory for all CMIS compliant devices. Other parts are only available for paged memory modules, or when advertised by the module. See CMIS V4.0 for details regarding the advertisement of supported management memory spaces.

In particular, support of the Lower Memory and of Page 00h is required for all modules, including passive copper cables. These pages are therefore always implemented. Additional support for Pages 01h, 02h and bank 0 of Pages 10h and 11h is required for all paged memory modules.

Bank 0 of pages 10h-1Fh, provides lane-specific registers for the first 1 lanes, and each additional bank provides support for additional 1 lanes. Note, however, that the allocation of information over the banks may be page specific and may not to be related to grouping data for 1 lanes.

The structure allows address space expansion for certain types of modules by allocating additional Pages. Moreover, additional banks of pages.



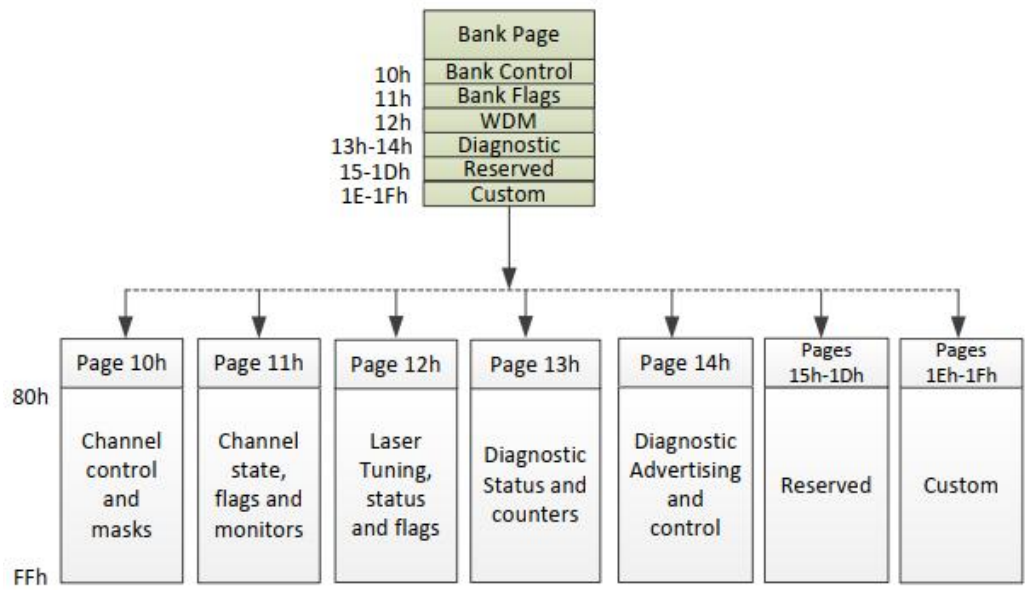


Figure 2. SFP112 Memory Map

Pin Definitions

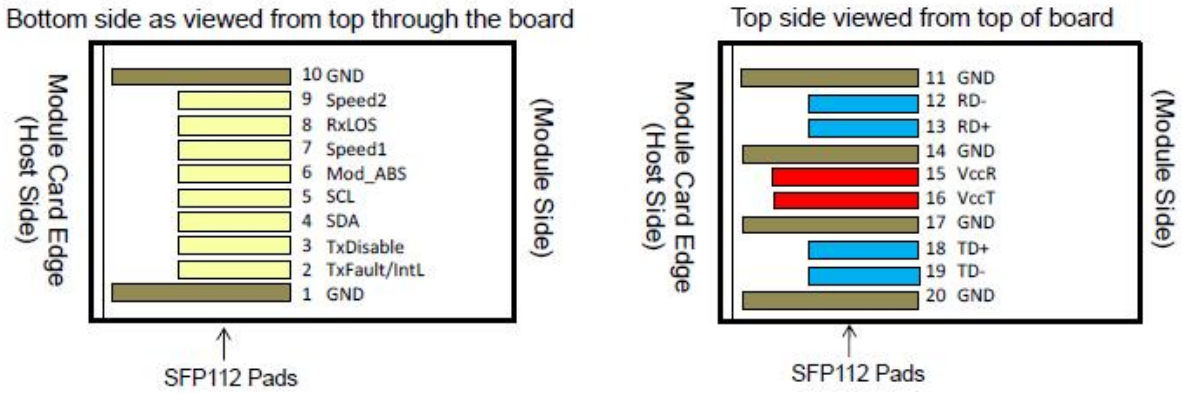


Figure 3. Pin View

Pin Descriptions

PIN	Logic	Symbol	Name / Description	Note
1		GND	Module Transmitter Ground	1
2	LVTTL-O	TxFault/IntL	Module Transmitter Fault (Default setting indicates TxFault, but optionally can be configured as IntL through CMIS.)	2
3	LVTTL-I	TxDisable	Transmitter Disable; Turns off transmitter laser output	
4	LVTTL-I/O	SDA	2-Wire Serial Interface Data Line	2
5	LVTTL-I	SCL	2-Wire Serial Interface Clock	2
6		Mod_ABS	Module Definition, Grounded in the module	
7	LVTTL-I	Speed1	Receiver Rate Select	
8	LVTTL-O	RX_LOS	Receiver Loss of Signal Indication Active LOW	
9	LVTTL-I	Speed2	Transmitter Rate Select (not used)	
10		GND	Module Receiver Ground	1
11		GND	Module Receiver Ground	1
12	CML-O	RD-	Receiver Inverted Data Output	
13	CML-O	RD+	Receiver Data Output	
14		GND	Module Receiver Ground	1
15		VccR	Module Receiver 3.3 V Supply	
16		VccT	Module Receiver 3.3 V Supply	
17		GND	Module Transmitter Ground	1
18	CML-I	TD+	Transmitter Non-Inverted Data Input	
19	CML-I	TD-	Transmitter Inverted Data Input	
20		GND	Module Transmitter Ground	1

Notes:

1. Module ground pins GND are isolated from the module case. 2. Shall be pulled up with 4.7K-10Kohms to a voltage between 3.15V and 3.45V on the host board.

Recommended Host Board Power Supply Filtering

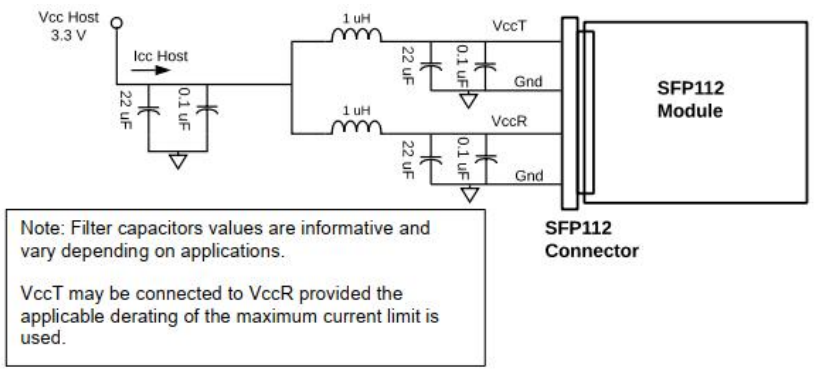


Figure 4. Host Board Power Supply Filtering

Recommended Interface Circuit

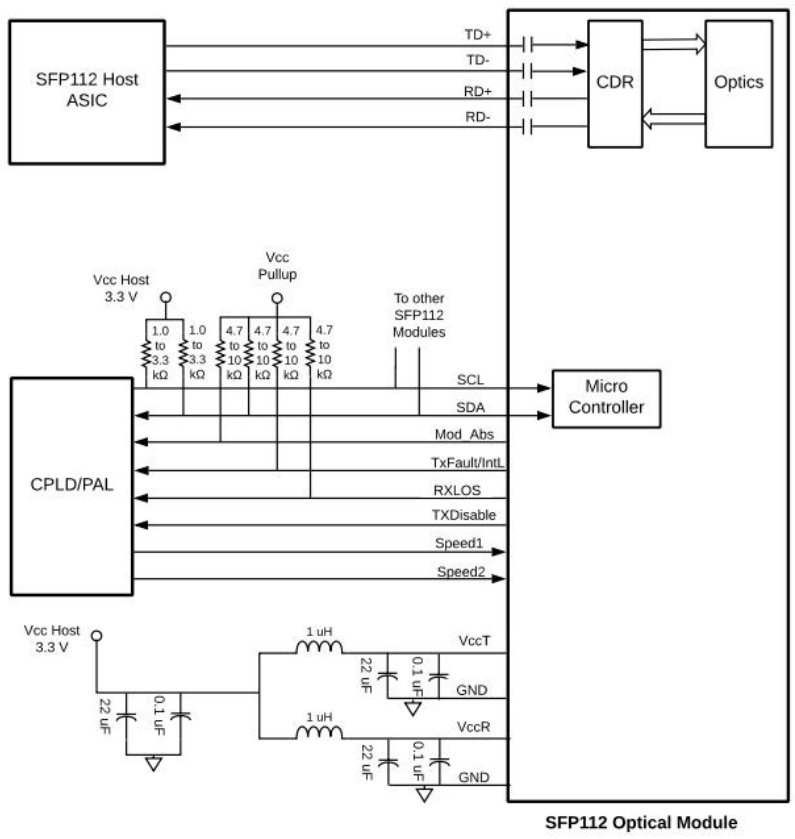
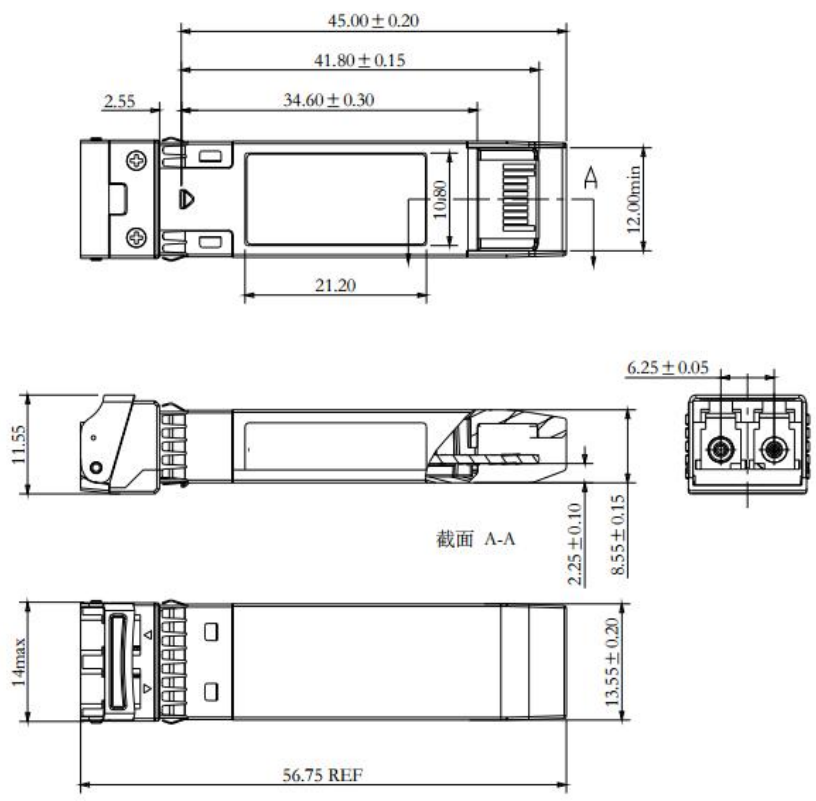


Figure5. Recommended Interface Circuit

Mechanical Dimensions



Regulatory Compliance

Fiberstamp GSS-SPO101-LR1C transceivers are Class 1 Laser Products. They meet the requirements of the following standards：

Feature	Standard
Laser Safety	IEC 60825-1:2014 (3rd Edition) IEC 60825-2:2004/AMD2:2010 EN 60825-1-2014
Electrical Safety	EN 62368-1: 2014 IEC 62368-1:2014

Environmental protection	Directive 2011/65/EU with amendment(EU)2015/863
CE EMC	EN55032：2015 EN55035：2017 EN61000-3-2:2014 EN61000-3-3:2013
FCC	FCC Part 15, Subpart B ANSI C63.4-2014

References

1. SFP112 MSA
2. CMIS
3. IEEE802.3cu 100GBASE-LR1
4. 100G Lambda MSA 100G LR1-10

⚠CAUTION:

Use of controls or adjustment or performance of procedures other than those specified herein may result in hazardous radiation exposure.

Ordering information

Part Number	Product Description
FSS-SPO101-LR1C	SFP112 LR1, 53.125GBd PAM4, 10km, EML+PIN, SMF, Dual LC, DDM, 0°C ~ +70°C

Important Notice

Performance figures,data and any illustrative material provided in this data sheet are typical and must be specifically confirmed in writing by Fiberstamp before they become applicable to any particular order or contract. In accordance with the Fiberstamp policy of continuous improvement specifications may change without notice.

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Revision History

Revision	Date	Description
V0	NOV-27-2024	Advance Release.