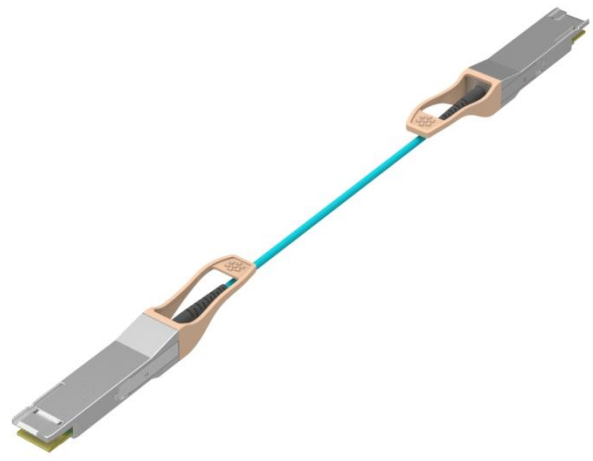
200GBASE-SR4 QSFP-DD Active Optical Cable

FYL-200MxxxC

Features

- 8 channels full-duplex transceiver modules
- Transmission data rate up to 26Gbps per channel
- Compliant with QSFP-DD MSA V5.0 and CMIS V4.0
- 8 channels 850nm VCSEL array
- 8 channels PIN photo detector array
- Internal CDR circuits on both receiver and transmitter channels
- Support CDR bypass
- Low power consumption <4W
- Hot Pluggable QSFP DD form factor
- Maximum link length of 70m on OM3 Multimode Fiber (MMF)and 100m on OM4 MMF
- MPO24 connector receptacle
- Built-in digital diagnostic functions
- Operating case temperature 0°C to +70°C
- 3.3V power supply voltage
- RoHS 6 compliant(lead free)



Applications

- IEEE 802.3bm 100GBASE SR4

Description

The FIBERSTAMP Technologies FYL-200MxxxC is an Eight-Channels, Pluggable, Parallel, Fiber-Optic QSFP Double Density for 2x100 Gigabit Ethernet Applications. This transceiver is a high performance module for short-range multi-lane data communication and interconnection applications. It integrates eight data lanes in each direction with 8x25.78125Gbps bandwidth. Each lane can operates at 25.78125Gbps up to 70 m using OM3 fiber or 100 m using OM4 fiber. These modules are designed to operate over multimode fiber systems using a nominal wavelength of 850nm. The electrical interface uses a 76 contact edge type connector. The optical interface uses a 24 fiber MTP (MPO) connector. This module incorporates FIBERSTAMP Technologies proven circuit and VCSEL technology to provide reliable long life, high performance, and consistent service.

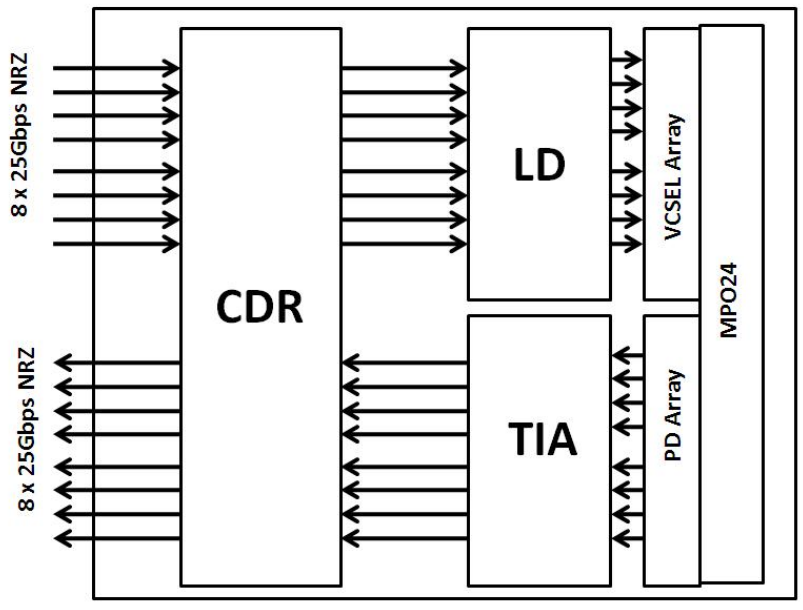


Figure 1. Module Block Diagram

The 2x100GBASE-SR4 QSFP DD is one kind of parallel transceiver. VCSEL and PIN array package is key technique, through I2C system can contact with module.

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{cc}	-0.3	3.6	V
Input Voltage	V_{in}	-0.3	Vcc+0.3	V
Storage Temperature	T_s	-20	85	℃
Case Operating Temperature	T_c	0	70	℃
Humidity (non-condensing)	Rh	5	95	%

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage	V_{cc}	3.13	3.3	3.47	V
Operating Case Temperature	T_c	0		70	℃
Data Rate Per Lane	fd		25.78125		Gbps
Humidity	Rh	5		85	%
Power Dissipation	P_m			4	W
Fiber Bend Radius	R_b	3			cm

Electrical Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Differential Input Impedance	Z_{in}	90	100	110	ohm
Differential Output Impedance	Z_{out}	90	100	110	ohm
Differential Input Voltage Amplitude[1]	ΔV_{in}	300		1100	mVp-p
Differential Output Voltage Amplitude[2]	ΔV_{out}	500		800	mVp-p
Skew	Sw			300	ps
Bit Error Rate	BER			5E-5	

Parameter	Symbol	Min	Typical	Max	Unit
Input Logic Level High	V_{IH}	2.0		VCC	V
Input Logic Level Low	V_{IL}	0		0.8	V
Output Logic Level High	V_{OH}	VCC-0.5		VCC	V
Output Logic Level Low	V_{OL}	0		0.4	V

Note:

1. BER=5E-5; PRBS 2^31-1@25.78125Gbps. Pre-FEC
2. Differential input voltage amplitude is measured between TxnP and TxnN
3. Differential output voltage amplitude is measured between RxnP and RxnN.

Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit
Transmitter					
Center Wavelength	λc	840	850	860	nm
RMS Spectral Width	Δλ	-	-	0.6	nm
Average Launch Power (each lane)	P_{out}	-8.4	-	2.4	dBm
Optical Modulation Amplitude (each lane)	OMA	-6.4		3	dBm
Transmitter and Dispersion Eye Closure (each lane)	TDEC			4.3	dB
Extinction Ratio	ER	3	-	-	dB
Average Launch Power of OFF Transmitter (each lane)	P_{off}			-30	dB
Eye Mask Coordinates[1]:X1, X2, X3, Y1, Y2, Y3	{0.3, 0.38, 0.45, 0.35, 0.41, 0.5}				
Receiver					
Center Wavelength	λ_C	840	850	860	nm
Stressed Receiver Sensitivity in OMA[2]				-5.2	dBm
Average Power at Receiver Input (each lane)		-10.3		2.4	dBm
Receiver Reflectance	R_R			-12	dB
LOS Assert	LOS_A	-30			dBm
LOS De-Assert – OMA	LOS_D			-7.5	dBm
LOS Hysteresis	LOS_H	0.5			dB

Note:

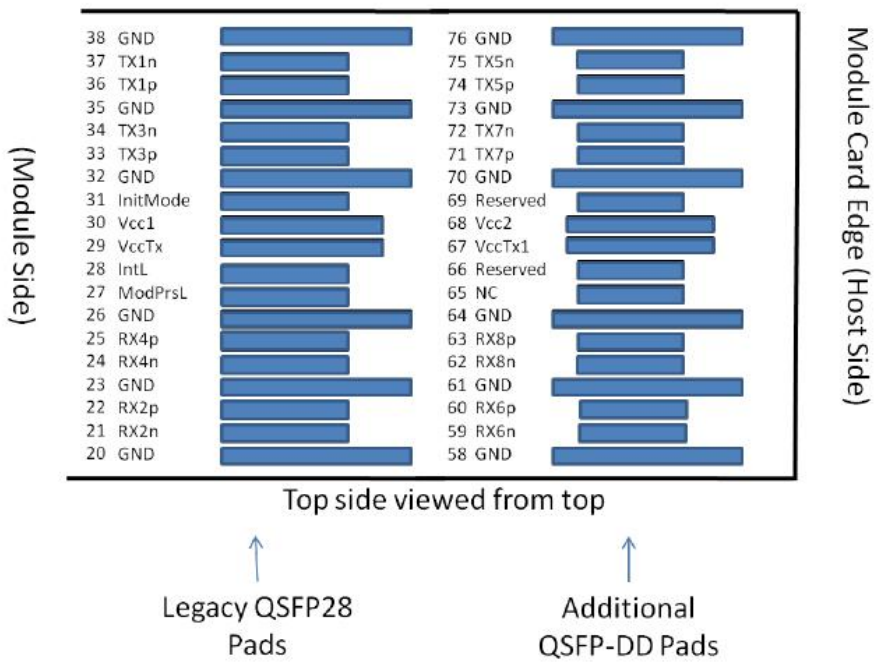
1. Hit Ratio = 5×10^{-5}
2. Measured with conformance test signal at TP3 for BER=5E-5

Pin Description

Pin	Logic	Symbol	Name/Description
1		GND	Module Ground[1]
2	CML-I	Tx2-	Transmitter inverted data input
3	CML-I	Tx2+	Transmitter non-inverted data input

Pin	Logic	Symbol	Name/Description
4		GND	Module Ground[1]
5	CML-I	Tx4-	Transmitter inverted data input
6	CML-I	Tx4+	Transmitter non-inverted data input
7		GND	Module Ground[1]
8	LVTTL-I	MODSEIL	Module Select[2]
9	LVTTL-I	ResetL	Module Reset[2]
10		VCCRx	+3.3V Receiver Power Supply
11	LVCMOS-I/O	SCL	2-wire Serial interface clock[2]
12	LVCMOS-I/O	SDA	2-wire Serial interface data[2]
13		GND	Module Ground[1]
14	CML-O	RX3+	Receiver non-inverted data output
15	CML-O	RX3-	Receiver inverted data output
16		GND	Module Ground[1]
17	CML-O	RX1+	Receiver non-inverted data output
18	CML-O	RX1-	Receiver inverted data output
19		GND	Module Ground[1]
20		GND	Module Ground[1]
21	CML-O	RX2-	Receiver inverted data output
22	CML-O	RX2+	Receiver non-inverted data output
23		GND	Module Ground[1]
24	CML-O	RX4-	Receiver inverted data output
25	CML-O	RX4+	Receiver non-inverted data output
26		GND	Module Ground[1]
27	LVTTL-O	ModPrsL	Module Present, internal pulled down to GND
28	LVTTL-O	IntL	Interrupt output, should be pulled up on host board[2]
29		VCCTx	+3.3V Transmitter Power Supply
30		VCC1	+3.3V Power Supply
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE
32		GND	Module Ground[1]
33	CML-I	Tx3+	Transmitter non-inverted data input
34	CML-I	Tx3-	Transmitter inverted data input
35		GND	Module Ground[1]
36	CML-I	Tx1+	Transmitter non-inverted data input
37	CML-I	Tx1-	Transmitter inverted data input
38		GND	Module Ground[1]

Pin	Logic	Symbol	Name/Description
39		GND	Module Ground[1]
40	CML-I	Tx6-	Transmitter inverted data input
41	CML-I	Tx6+	Transmitter non-inverted data input
42		GND	Module Ground[1]
43	CML-I	Tx8-	Transmitter inverted data input
44	CML-I	Tx8+	Transmitter non-inverted data input
45		GND	Module Ground
46		Reserved	For future use
47		VS1	Module Vender Specific 1
48		VCCRx1	+3.3V Power Supply
49		VS2	Module Vender Specific 2
50		VS3	Module Vender Specific 3
51		GND	Module Ground
52	CML-O	RX7+	Receiver non-inverted data output
53	CML-O	RX7-	Receiver inverted data output
54		GND	Module Ground
55	CML-O	RX5+	Receiver non-inverted data output
56	CML-O	RX5-	Receiver inverted data output
57		GND	Module Ground
58		GND	Module Ground
59	CML-O	RX6-	Receiver inverted data output
60	CML-O	RX6+	Receiver non-inverted data output
61		GND	Module Ground
62	CML-O	RX8-	Receiver inverted data output
63	CML-O	RX8+	Receiver non-inverted data output
64		GND	Module Ground
65		NC	N0 Connect
66		Reserved	For future use
67		VCCTx1	+3.3V Power Supply
68		VCC2	+3.3V Power Supply
69		Reserved	For future use



Pin	Logic	Symbol	Name/Description
70		GND	Module Ground[1]
71	CML-I	Tx7+	Transmitter non-inverted data input
72	CML-I	Tx7-	Transmitter inverted data input
73		GND	Module Ground[1]
74	CML-I	Tx5+	Transmitter non-inverted data input
75	CML-I	Tx5-	Transmitter inverted data input
76		GND	Module Ground

Note:

1. Module circuit ground is isolated from module chassis ground within the module.
2. Open collector should be pulled up with 4.7K to 10K ohms on host board to a voltage between 3.15V and 3.6V.

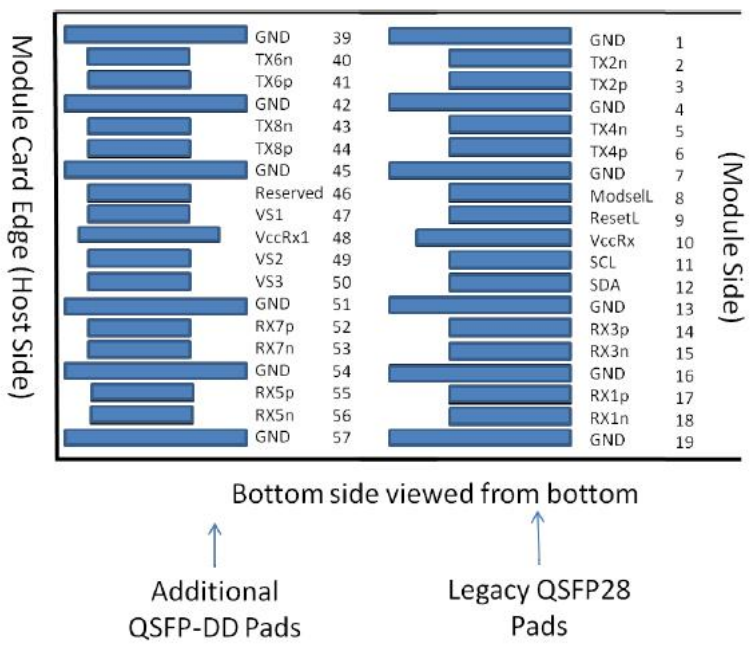


Figure 2. Electrical Pin-out Details

ModSelL Pin

The ModSelL is an input signal that must be pulled to Vcc in the QSFP-DD module. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP-DD modules on a single 2-wire interface bus. When ModSelL is "High", the module shall not respond to or acknowledge any 2-wire interface communication from the host.

In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the ModSelL de-assert time after any QSFP-DD modules are deselected. Similarly, the host must wait at least for the period of the ModSelL assert time

before communicating with the newly selected module. The assertion and de-asserting periods of different modules may overlap as long as the above timing requirements are met.

ResetL Pin

The ResetL signal shall be pulled to Vcc in the module. A low level on the ResetL signal for longer than the minimum pulse length (t_Reset_init) (See Table 13) initiates a complete module reset, returning all user module settings to their default state.

InitMode Pin

InitMode is an input signal. The InitMode signal must be pulled up to Vcc in the QSFP-DD module. The InitMode signal allows the host to define whether the QSFP-DD module will initialize under host software control (InitMode asserted High) or module hardware control (InitMode deasserted Low). Under host software control, the module shall remain in Low Power Mode until software enables the transition to High Power Mode, as defined in Section 7.5. Under hardware control (InitMode de-asserted Low), the module may immediately transition to High Power Mode after the management interface is initialized. The host shall not change the state of this signal while the module is present. In legacy QSFP applications, this signal is named LPMode. See SFF-8679 for signal description.

ModPrsL Pin

ModPrsL must be pulled up to Vcc Host on the host board and grounded in the module. The ModPrsL is asserted “Low” when the module is inserted and deasserted “High” when the module is physically absent from the host connector.

IntL Pin

IntL is an output signal. The IntL signal is an open collector output and must be pulled to Vcc Host on the host board. When the IntL signal is asserted Low it indicates a change in module state, a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL signal is deasserted “High” after all set interrupt flags are read.

Power Supply Filtering

The host board should use the power supply filtering shown in Figure 3.

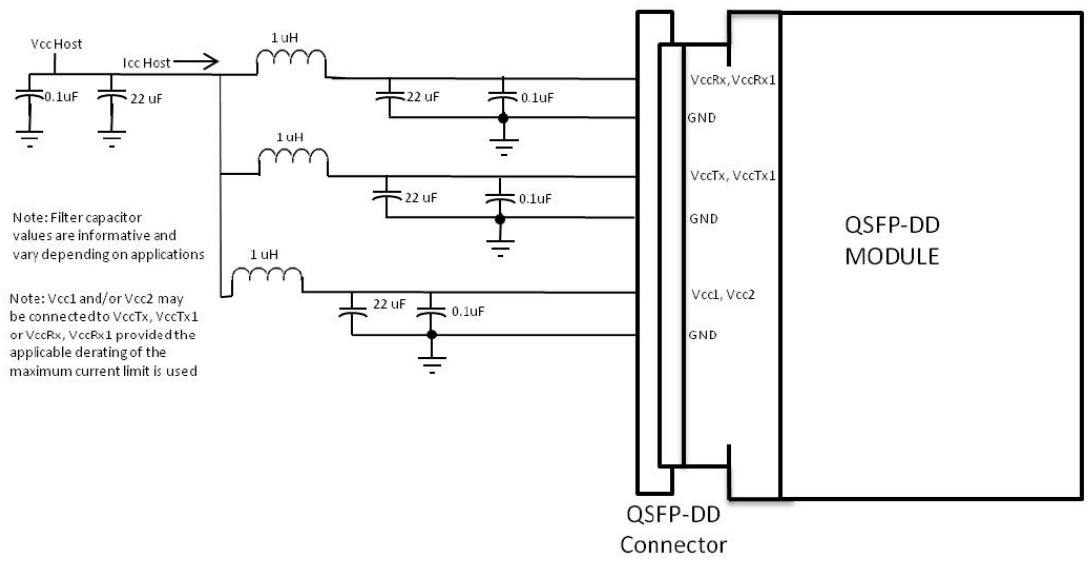


Figure 3. Host Board Power Supply Filtering

Optical Interface Lanes and Assignment

The optical interface port is a male MPO connector .The eight fiber positions on the left as shown in Figure 4, with the key up, are used for the optical transmit signals (Channel 1 through 8). The fiber positions on the right are used for the optical receive signals (Channel 8 through 1). The central eight fibers are physically present.

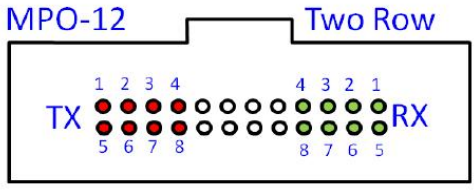


Figure 4. Optical Receptacle and Channel Orientation

DIAGNOSTIC MONITORING INTERFACE(OPTIONAL)

Digital diagnostics monitoring function is available on all FIBERSTAMP QSFP DD products. A 2-wire serial interface provides user to contact with module.

The structure of the memory is shown in Figure 5. The memory space is arranged into a lower, single page, address space of 128 bytes and multiple upper address space pages. This structure permits timely access to addresses in the lower page, e.g. Interrupt Flags and Monitors. Less time critical entries, e.g. serial ID information and threshold setting, are available with the Page Select function. The structure also provides address expansion by adding additional upper pages as needed.

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The interface address used is A0xh and is mainly used for time critical data like interrupt handling in order to enable a one-time-read for all data related to an interrupt situation. After an interrupt, IntL, has been asserted, the host can read out the flag field to determine the affected channel and type of flag.

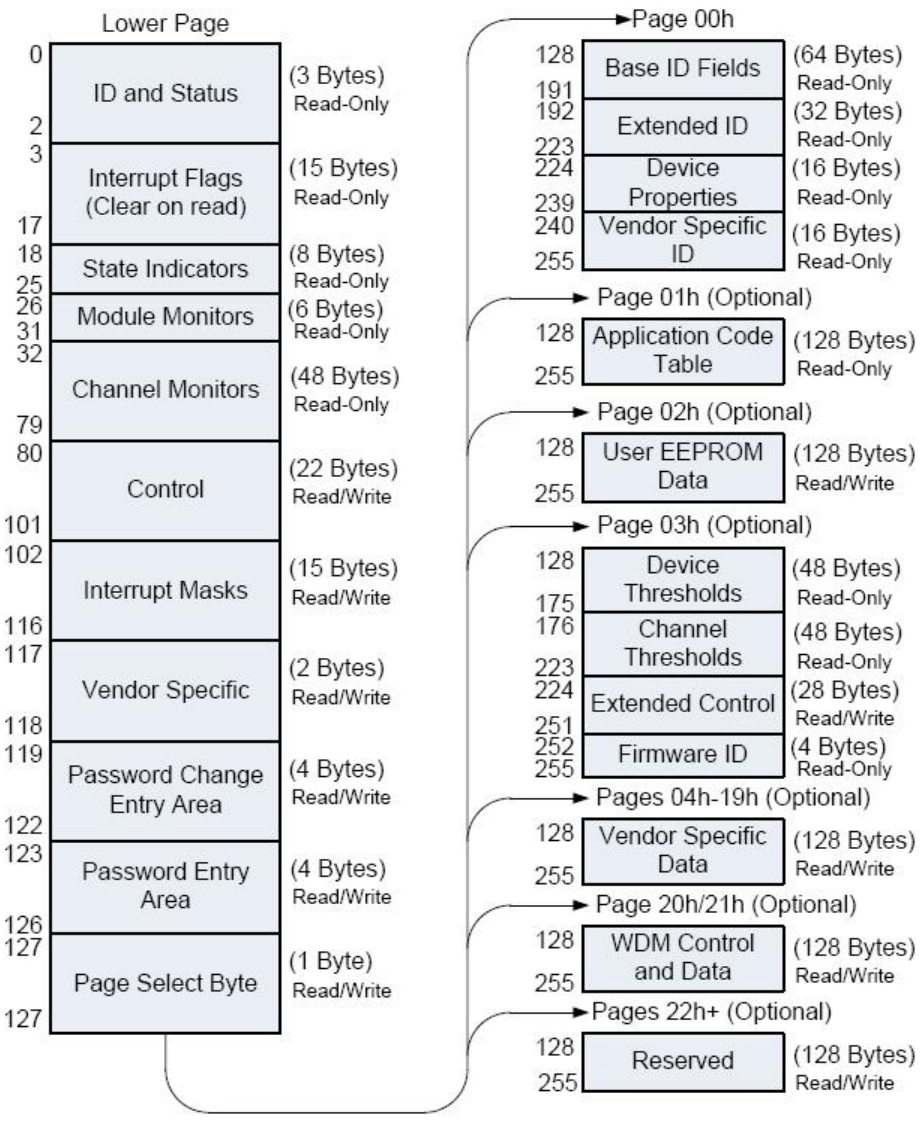

Figure 5. QSFP DD Memory Map

Table 16- Lower Page Overview (Lower Page)

Address	Description	Type
0 – 2	Id and Status (3 bytes)	Read-only
3 – 17	Interrupt Flags (15 bytes)	Read-only
18 – 25	State Indicators (8 bytes)	Read-only
26 – 31	Module card Monitors (6 bytes)	Read-only
32 – 79	Channel Monitors (48 bytes)	Read-only
80 – 101	Control Fields (22 bytes)	Read/Write
102 – 116	Interrupt Flag Masks (15 bytes)	Read/Write
117 – 118	Reserved	Read/Write
119 – 122	Password Change Area (4 bytes)	Write-Only
123 – 126	Password Entry Area (4 bytes)	Write-Only
127	Page Select Byte	Read/Write

Figure 6. Low Memory Map

Byte Address	Description	Type
128-175	Module Thresholds (48 Bytes)	Read Only
176-223	Reserved (48 Bytes)	Read Only
224-225	Reserved (2 Bytes)	Read Only
226-239	Reserved (14 Bytes)	Read/Write
240-241	Channel Controls (2 Bytes)	Read/Write
242-253	Reserved (12 Bytes)	Read/Write
254-255	Reserved (2 Bytes)	Read/Write

Figure 7. Page 03 Memory Map

Table 28- Upper Page 0 Overview (Page 00h)

Address	Size (bytes)	Name	Description
Base ID Fields:			
128	1	Identifier	Identifier Type of module
129	1	Ext. Identifier	Extended Identifier
130	1	Connector Type	Code for media connector type
131-138	8	Specification compliance	Code for electronic compatibility or optical compatibility
139	1	Encoding	Code for serial encoding algorithm
140	1	BR, nominal	Nominal bit rate, units of 100 MBits/s
141	1	Extended rate select compliance	Tags for extended rate select compliance
142-146	5	Link length	Link length / transmission media
147	1	Device technology	Device technology
148-163	16	Vendor name	Vendor name (ASCII)
164	1	Extended Module	Extended Module codes for InfiniBand
165-167	3	Vendor OUI	Vendor IEEE company ID
168-183	16	Vendor PN	Part number provided by vendor (ASCII)
184-185	2	Vendor rev	Revision level for part number provided by vendor (ASCII)
186-187	2	Wavelength or Copper cable Attenuation	Nominal laser wavelength (wavelength=value/20 in nm) or copper cable attenuation in dB at 2.5GHz (Adrs 186) and 5.0GHz (Adrs 187)
188-189	2	Wavelength tolerance	Guaranteed range of laser wavelength(+/- value) from nominal wavelength.(wavelength Tolerance=value/200 in nm)
190	1	Max case temp.	Maximum case temperature in degrees C
191	1	CC_BASE	Check code for base ID fields (addresses 128-190 inclusive)
Extended ID Fields:			
192-195	4	Options	Indicates which optional capabilities are implemented in the module
196-211	16	Vendor S/N	Vendor product serial number
212-219	8	Date Code	Vendor's manufacturing date code
220	1	Diagnostic Monitoring Type	Indicates which types of diagnostic monitoring are implemented in the module
221-222	2	Enhanced Options	Indicates which optional enhanced features are implemented in the module.
223	1	CC_EXT	Check code for the Extended ID Fields (addresses 192-222 inclusive)
224-238	15	Device Properties	Provides detailed information about the device
239	1	CC-PROP	Check code for the Device Properties Fields (addresses 224-2382 inclusive)
Vendor Specific ID Fields:			
240-255	16	Vendor-Specific	Vendor-specific ID information

Figure 8. Page 00 Memory Map

Page02 is User EEPROM and its format decided by user.

The detail description of low memory and Page 00, Page 03 upper memory, please see SFF-8436 document.

Timing for Soft Control and Status

Table 13- Timing for QSFP-DD soft control and status functions

Parameter	Symbol	Min	Max	Unit	Conditions
MgmtInitDuration	Max MgmtInit Duration		2000	ms	Time from power on[2] , hot plug or rising edge of reset until completion of the MgmtInit State
ResetL Assert Time	t_reset_init	2		µs	Minimum pulse time on the ResetL signal to initiate a module reset.
IntL Assert Time	ton_IntL		200	ms	Time from occurrence of condition triggering IntL until Vout:IntL=Vol
IntL Deassert Time	toff_IntL		500	µs	Time from clear on read[3] operation of associated flag until Vout:IntL=Voh. This includes deassert times for Rx LOS, Tx Fault and other flag bits.
Rx LOS Assert Time	ton_los		100	ms	Time from Rx LOS state to Rx LOS bit set (value = 1b) and IntL asserted.
Rx LOS Assert Time (optional fast mode)	ton_losf		1	ms	Time from Rx LOS state to Rx LOS bit set (value = 1b) and IntL asserted.
Rx LOS Deassert Time (optional fast mode)	toff_losf		3	ms	Time from signal present to negation of Rx LOS status bit.
Tx Fault Assert Time	ton_Txfault		200	ms	Time from Tx Fault state to Tx Fault bit set (value=1b) and IntL asserted.
Flag Assert Time	ton_flag		200	ms	Time from occurrence of condition triggering flag to associated flag bit set (value=1b) and IntL asserted.
Mask Assert Time	ton_mask		100	ms	Time from mask bit set (value=1b)[1] until associated IntL assertion is inhibited
Mask Deassert Time	toff_mask		100	ms	Time from mask bit cleared (value=0b)[1] until associated IntL operation resumes
Application or Rate Select Change Time	t_ratesel		100	ms	Time from change of state of Application or Rate Select bit[1] until transmitter or receiver bandwidth is in conformance with appropriate specification
Note 1. Measured from the rising edge of SDA in the stop bit of the write transaction					
Note 2. Power on is defined as the instant when supply voltages reach and remain at or above the minimum level specified in Table 6.					
Note 3. Measured from the rising edge of SDA in the stop bit of the read transaction					

Functions

Mechanical Dimensions

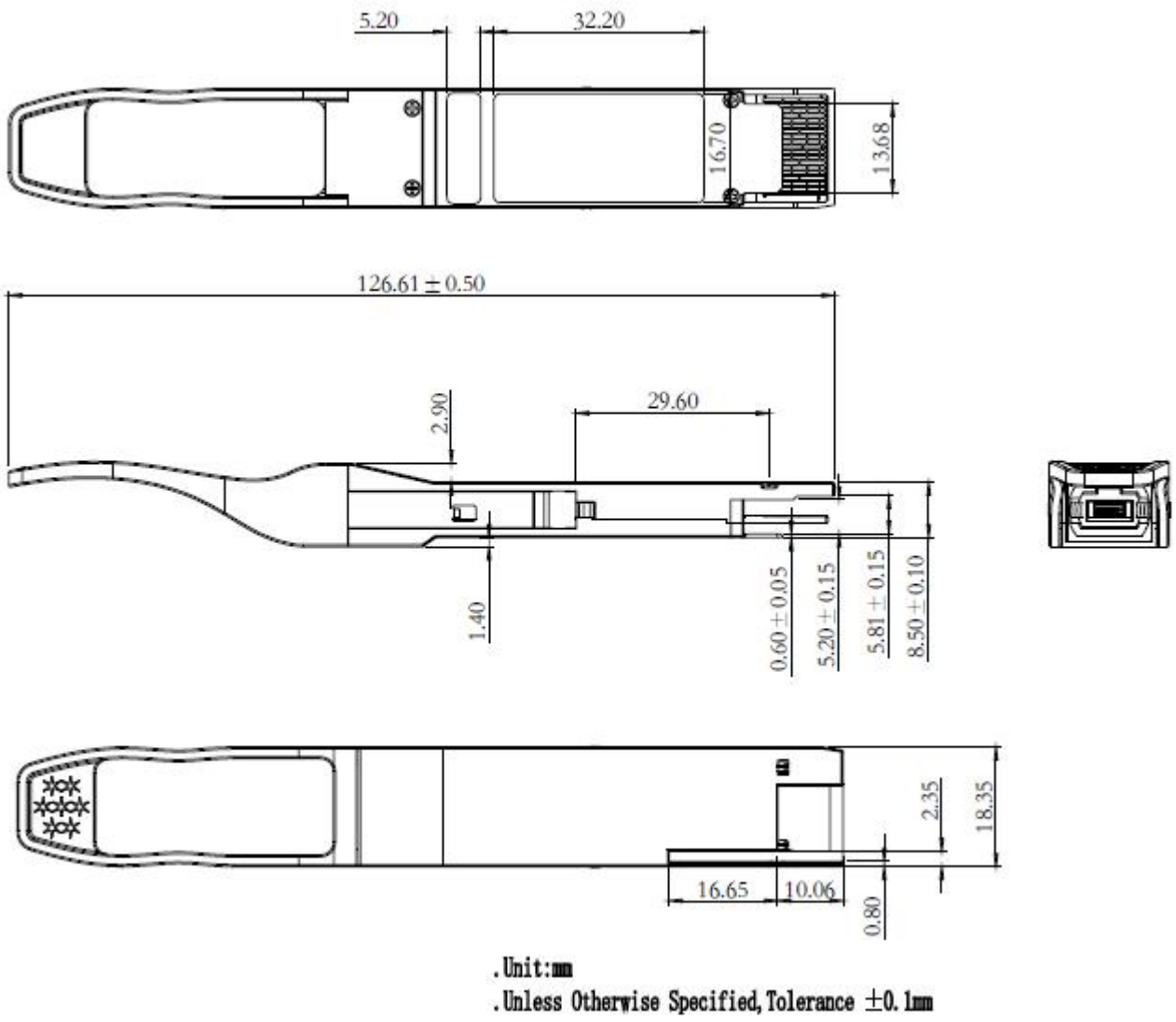

Figure 9. Mechanical Specifications

Regulatory Compliance

FIBERSTAMP FYL-200MxxxC AOC are Class 1 Laser Products. They are certified per the following standards:

Feature	Agency	Standard
Laser Eye Safety	FDA/CDRH	CDRH 21 CFR 1040 and Laser Notice 50
Laser Eye Safety	TÜV	EN 60825-1:2007 EN 60825-2:2004+A1+A2
Electrical Safety	TÜV	EN 60950
Electrical Safety	UL/CSA	CLASS 3862.07 CLASS 3862.87

Complies with FDA performance standards for laser products except for deviations pursuant to Laser Noticed No. 50, dated June 24, 2007.

References

1. QSFP-DD MSA Rev5.0
2. Ethernet 100GBASE-SR4 IEEE802.3bm
3. Directive 2011/65/EU of the European Parliament and of the Council, "on the restriction of the use of certain hazardous substances in electrical and electronic equipment," July 1, 2011.

⚠CAUTION:

Use of controls or adjustment or performance of procedures other than those specified herein may result in hazardous radiation exposure.

Ordering Information

Part Number	Product Description
FYL-200MxxxC	2x100GBASE-SR4 QSFP-DD Active Optical Cable, xxx is length of fiber cable, up to 70m on OM3 Multimode Fiber (MMF) and up to 100m on OM4 MMF.

Important Notice

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